

Fig. 1

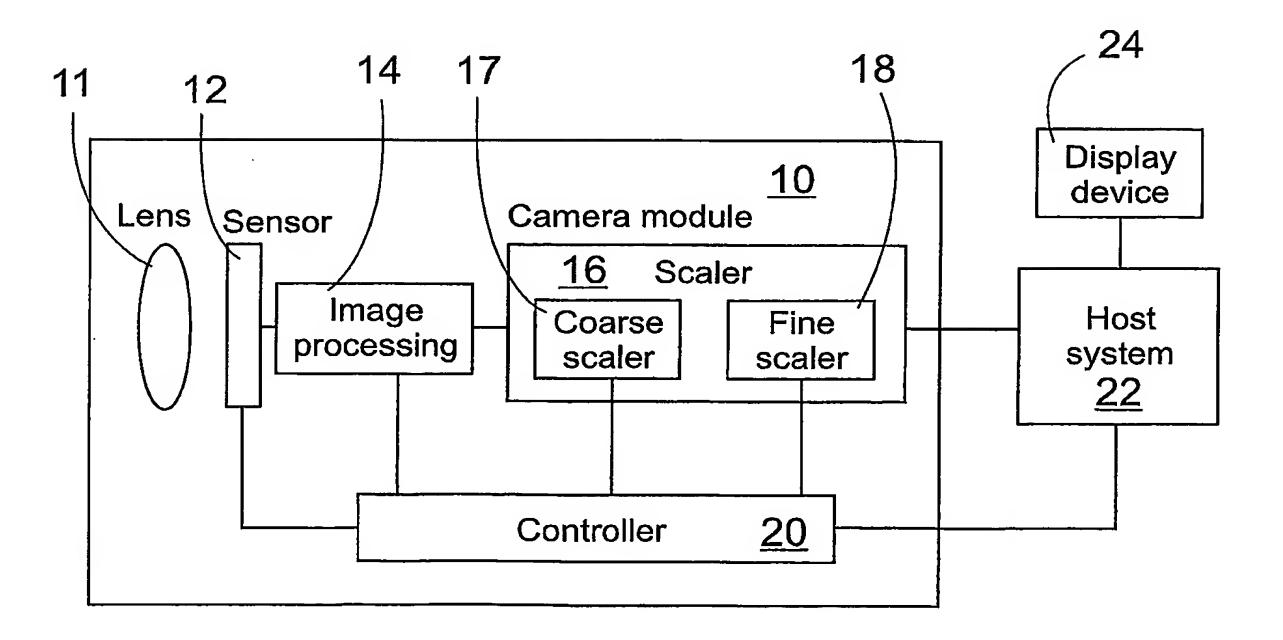


Fig. 2a

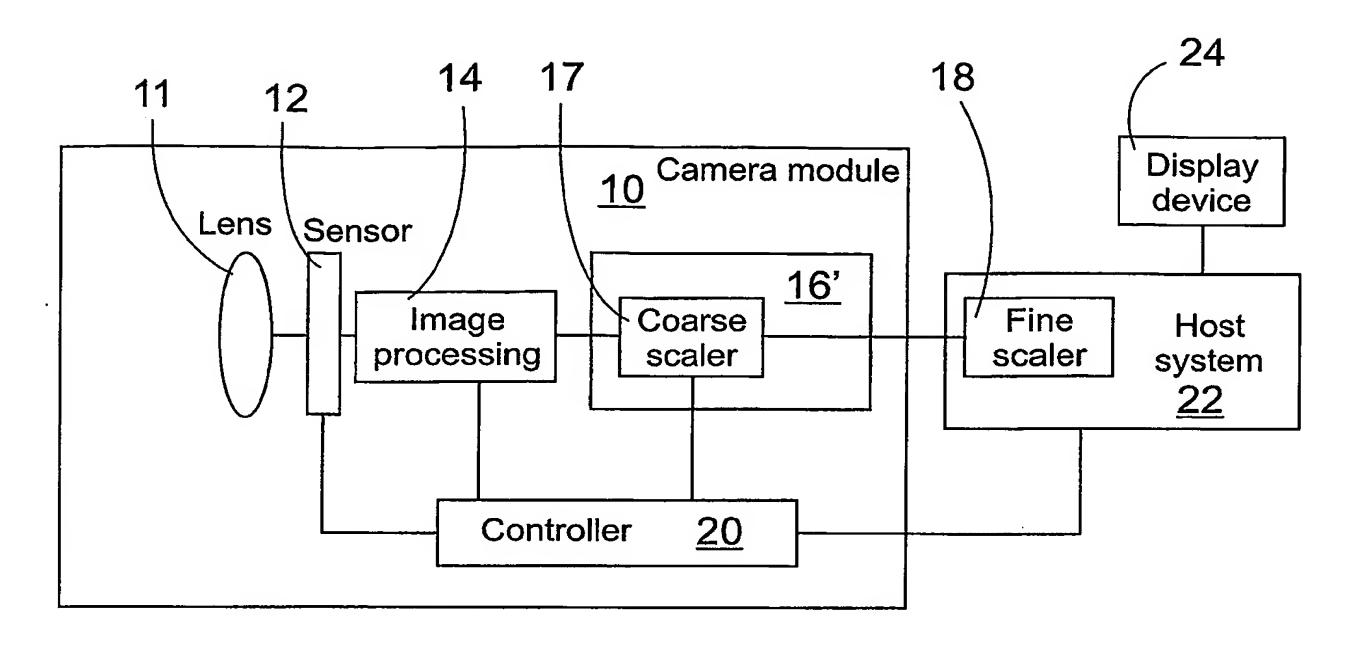
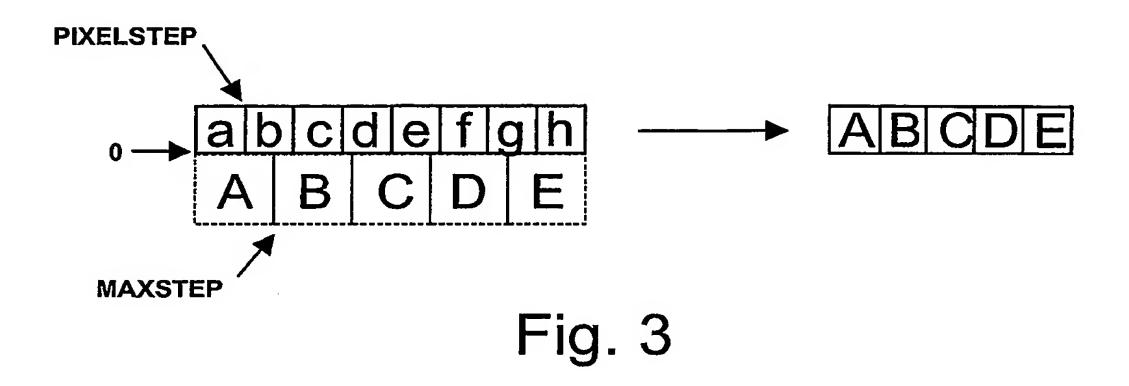
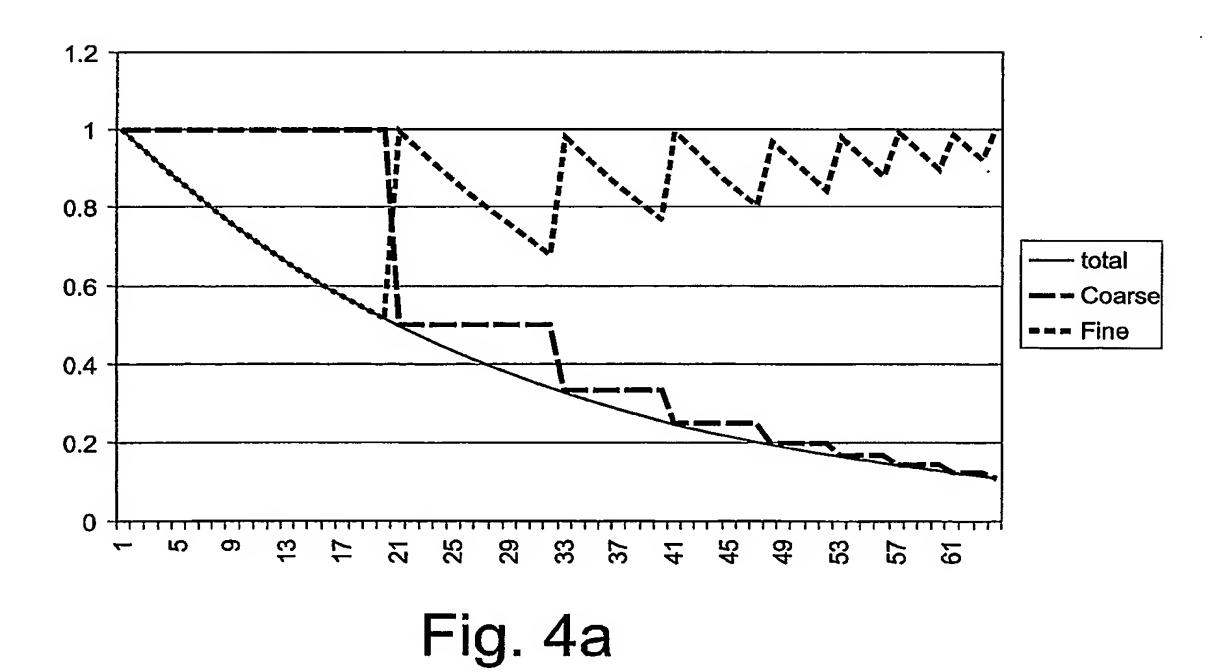


Fig. 2b 18 16' 163 162 183 <u>10</u> Host system <u>22</u> 182 CPU Memory [→]Memory CPU Input unit Input unit G Doutput Cutput 184 Control Control 181 164 161 165 185 187 167

Fig. 2c





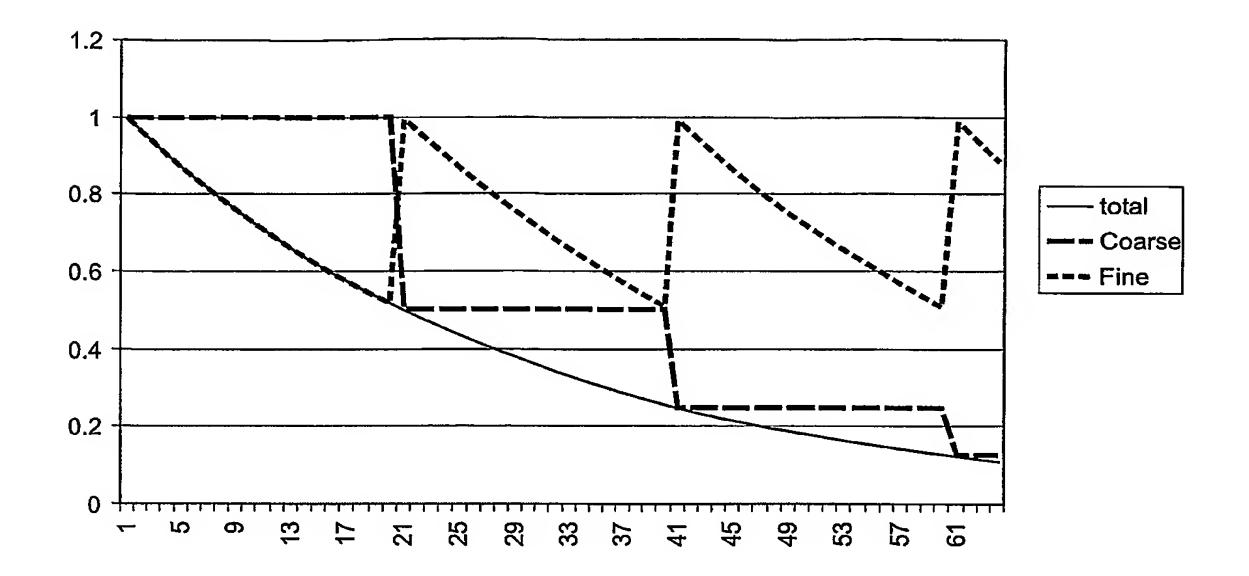


Fig. 4b

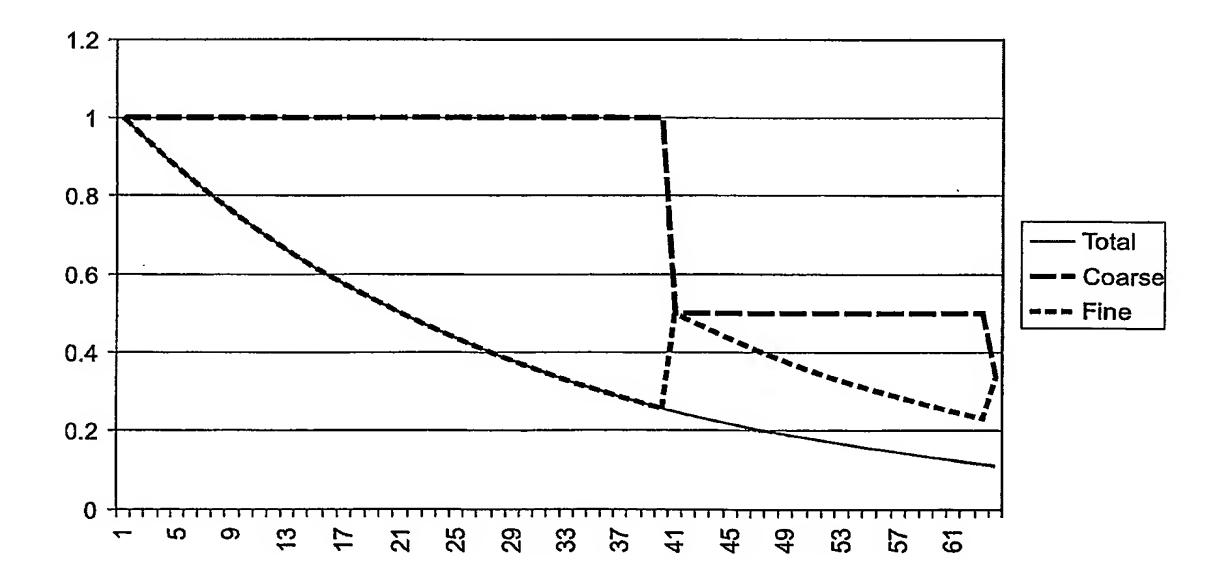


Fig. 4c